ABSTRACT OF THE DISCLOSURE

An apparatus and method in a pipelined microprocessor for selecting one of a plurality of branch target addresses cached in a branch target address cache (BTAC) within a line selected by an instruction cache fetch address. The invention enables support for speculatively branching to one of a plurality of branch instructions potentially cached in an instruction cache line selected by the fetch address. Each target address has cached with it in the BTAC an associated offset within the instruction cache line of the previously executed associated branch instruction as well as a valid bit and a prediction of whether the branch instruction will be taken or not taken. Control logic selects the first, valid, taken, and seen target address. The target address is "seen" if the associated offset is greater than or equal to a corresponding portion of the least significant bits of the fetch address.